REMARKS

The application has been reviewed in light of the Office Action dated October 26, 2005. Claims 1-19 were pending. By this Amendment, new claim 20 has been added. Accordingly, claims 1-20 are now pending, with claims 1, 10 and 19 being in independent form.

Claims 19 was rejected under 35 U.S.C. § 102(e) as purportedly anticipated by U.S. Patent No. 6,799,242 to Tsuda et al. Claims 1-3, 7, 9-12, 16 and 18 were rejected under 35 U.S.C. § 103(a) as purportedly obvious over Tsuda in view of U.S. Patent No. 6,373,598 to Matsumoto et al. Claims 4-6, 8, 13-15 and 17 were rejected under 35 U.S.C. § 103(a) as purportedly obvious over Tsuda in view of Matsumoto and further in view of U.S. Patent No. 6,470,439 to Yamada et al.

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1, 10 and 19 are patentable over the cited art, for at least the following reasons.

This application relates to a communications interfacing apparatus and method. Applicant devised improved apparatuses and methods for communications interfacing which can be used, for example, in an optical disk drive mechanism for interfacing communications of data between the optical disk drive mechanism and a host computer connected thereto.

For example, independent claim 1 is directed to a communications interface apparatus comprising a register circuit, a first memory, a second memory and a control circuit. The register circuit stores data to be transferred to a host computer. The first memory stores first information indicating a specific address of the register circuit and representing an access to the communications interface apparatus executed by the host computer for a data transfer. The second memory stores second information, sent from the host computer in association with the

first information stored in the first memory, to be written into the register circuit at the specific address indicated by the first information stored in the first memory. The control circuit is configured to perform an information writing operation for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed.

Claim 19 is directed to an optical disk drive apparatus comprising an optical disk drive mechanism and an interface circuit. The interface circuit interfaces communications between the optical disk drive mechanism and a host computer, and comprises an input terminal, a data processor, a clock generator, an operation mode changer and a buffering circuit block. The input terminal receives data sent from the host computer. The data processor is configured to perform a predetermined data processing operation to the data received through the input terminal from the host computer. The operation mode changer is configured to control the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode. The buffering circuit block is configured to buffer the data received through the input terminal from the host computer. The buffering circuit block includes a first data transfer path, a second data transfer path and a path selection controller. The first data transfer path is configured to transfer the data received through the input terminal from the host computer to the data processor not via a memory. The second data transfer path is configured to transfer the data received through the input terminal from the host computer to the data processor via a memory. The path selection controller controls the buffering circuit clock to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode.

Tsuda, as understood by Applicant, is directed to an optical disc player having a sleep mode.

The Office Action states that Tsuda discloses a host interface 13 for receiving data received from a host computer.

Applicant disagrees. Tsuda proposes that data is supplied from the optical disc player through the host interface to the host computer. Since Tsuda is concerned with reproduction of data from an optical disc, and not recording of data to the optical disc, it is unsurprising that Tsuda neither teaches nor suggests receiving data from the host computer through the host interface 13.

Fig. 7 of Tsuda shows a digital signal processor 250 and a CD-ROM decoder 260 proposed to be used in an optical disc player. Tsuda, column 7, lines 17-56, discusses operation of the digital signal processor 250 to process EFM data reproduced by the optical disc player from an optical disc.

Contrary to the contention in the Office Action, the digital signal processor 250 of Tsuda does not perform data processing operation to data received through an input terminal from a host computer.

Fig. 6 of Tsuda shows a CD-ROM decoder including a TOC (table of contents) data buffer RAM 132. Tsuda proposes that TOC data (such as index information which indicates what data is recorded at which position on the disc) read from an optical disc is stored in a TOC data buffer RAM 132. Thus, the TOC data is used by the optical disc player, but is transparent to, and certainly not received from, the host computer.

Contrary to the contention in the Office Action, the CD-ROM decoder of Tsuda does not buffer data from the host computer received through an input terminal.

Applicant simply does not find teaching or suggestion in Tsuda that data sent from the host computer is received by an optical disk drive apparatus through an input terminal of an interface circuit of the optical disk drive apparatus, or that such data is processed by a data processor, or that such data is buffered by a buffering circuit, as provided by claim 19 of the present application.

Regarding independent claims 1 and 10, it should be noted that buffer RAM 7 of Tsuda is proposed by Tsuda to store TOC data, and the address register 230 stores address of the TOC data in the buffer RAM 7. As mentioned above, TOC data is used by the optical disc player proposed by Tsuda and is not transferred to the host computer.

It should be noted that the microcomputer interface 244 of Tsuda interfaces with control microcomputer 244 which is a component of the optical disc player which performs control operations for the optical disc player, and is not a host computer.

Applicant does not find teaching or suggestion in Tsuda of storing in a register circuit data to be transferred to a host computer, storing in a first memory first information indicating a specific address of the register circuit and representing an access to a communications interface apparatus executed by the host computer for a data transfer, storing in a second memory second information, sent from the host computer in association with the first information stored in the first memory, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and performing an information writing operation with a control circuit for writing the first information into the first memory and the second information into the second memory in chronological order of accesses executed, as provided by each of independent claims 1 and 10 of the present application.

Matsumoto, as understood by Applicant, is directed to a facsimile machine for use in

combination with a personal computer connected to the facsimile machine. Matsumoto proposes using a hard disk of the personal computer, coupled with a storage device of the facsimile machine, to store the large amount of data for operating and managing the facsimile machine (such as control programs, facsimile transaction information, and help information for guiding a user to use the facsimile machine). Matsumoto was cited in the Office Action for its proposal of "a single control means for controlling a selected one of said first storage device and said second storage device to store facsimile transaction information".

Yamada, as understood by Applicant, is directed to a FIFO (first-in-first-out) memory control circuit, such as used in an electronic device, for performing asynchronous read/write control when a write clock and a read clock are different. Yamada was cited in the Office Action as purportedly proposing that the FIFO memory includes a specific number of buffer areas into which data from a host computer is written.

Amongst other deficiencies, Yamada does not disclose or suggest communication of data between the electronic device and a host computer.

Applicant simply does not find disclosure or suggestion in the cited art, however, of storing in a register circuit data to be transferred to a host computer, storing in a first memory first information indicating a specific address of the register circuit and representing an access to a communications interface apparatus executed by the host computer for a data transfer, storing in a second memory second information, sent from the host computer in association with the first information stored in the first memory, to be written into the register circuit at the specific address indicated by the first information stored in the first memory, and performing an information writing operation with a control circuit for writing the first information into the first memory and the second information into the second memory in chronological order of accesses

executed, as provided by each of independent claims 1 and 10 of the present application.

Likewise, Applicant does not find teaching or suggestion in the cited art of an optical disk drive apparatus comprising an interface circuit which interfaces communications between an optical disk drive mechanism and a host computer, and comprises an input terminal, a data processor, a clock generator, an operation mode changer and a buffering circuit block, wherein the input terminal receives data sent from the host computer, the data processor performs a predetermined data processing operation to the data received through the input terminal from the host computer, the operation mode changer controls the clock generator to reduce a frequency of the clock signal to a value smaller than a predetermined value to change an operation mode from a regular operation mode to a low power consumption mode, the buffering circuit block buffer the data received through the input terminal from the host computer and includes a first data transfer path, a second data transfer path and a path selection controller, the first data transfer path is configured to transfer the data received through the input terminal from the host computer to the data processor not via a memory, the second data transfer path is configured to transfer the data received through the input terminal from the host computer to the data processor via a memory, and the path selection controller controls the buffering circuit clock to select the second data transfer path on an exclusive basis when the operation mode is changed from the regular operation mode to the low power consumption mode, as provided by claim 19 of the present application.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1, 10 and 19, and the claims depending therefrom, are patentable over the cited art.

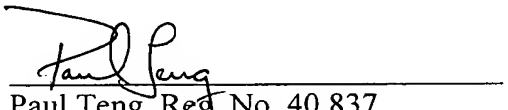
In view of the remarks hereinabove, Applicant submits that the application is now in

condition for allowance, and earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is respectfully requested to call the undersigned attorney.

Respectfully submitted,



Paul Teng, Reg. No. 40,837
Attorney for Applicant
Cooper & Dunham LLP
Tel.: (212) 278-0400